CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A system for coordinating channel bonding operations of a plurality of transceivers of an integrated circuit, comprising:

a master transceiver of the integrated circuit that performs channel bonding operations for aligning different portions of a data stream transmitted in parallel by way of a plurality of data channels;

a plurality of first level transceivers of the integrated circuit that perform channel bonding operations, each first level transceivers being controlled by the master transceiver and receiving a control signal by way of a first configurable path, wherein the first configurable path is configured according to a first mode signal for a first level transceiver, the first mode signal determining a delay of the control signal received by way of the first configurable path; and

a plurality of second level transceivers of the integrated circuit that perform channel bonding operations, each second level transceiver being controlled by one of the plurality of first level transceivers and receiving a control signal by way of a second configurable path, wherein the second configurable path is configured according to a second mode signal for a second level transceiver, the second mode signal determining a delay of the control signal received by way of the second configurable path;

wherein each transceiver comprises a controller receiving a mode control signal designating the transceiver as a master transceiver or a slave transceiver and enabling a control signal to be applied to the transceiver by way of a configurable path during a predetermined clock cycle to enable channel bonding operations for aligning the different portions of the data stream transmitted in parallel.

2. (Original) The system of claim 1 wherein each of the plurality of transceivers can be selected as either the master transceiver, one of the first level transceivers or one of the second level transceivers.

3. (Original) The system of claim 1 further comprising a clock signal, and wherein the master transceiver and the plurality of first level transceivers generate respective control signals at different cycles of the clock signal.

4. (Original) The system of claim 1 wherein each of the plurality of transceivers contains at least one buffer for the channel bonding operations.

5. (Previously Presented) An apparatus that generates an output signal in response to a first input signal and a second input signal comprising control signals for aligning data, the apparatus comprising:

a first flip-flop that accepts the first input signal and generate an output signal;

a first multiplexer having an output terminal and at least a first and a second input terminal, the first input terminal accepting the output signal of the first flip-flop, and the second input terminal being connected to the second input signal;

a second flip-flop having an output terminal and an input terminal that connects with the output terminal of the first multiplexer;

a second multiplexer having an output terminal and at least a first and a second input terminal, the first input terminal being connected to the output terminal of the second flip-flop, and the second input terminal being connected to the second input signal; and

a third flip-flop having an output terminal and an input terminal, the input terminal being connected to the output terminal of the second multiplexer.

6. (Previously Presented) The apparatus of claim 5 further comprising:

a third multiplexer having an output terminal and at least a first and a second input terminal, the first input terminal being connected to the first input signal, the second input terminal being connected to the second input signal; and

a fourth flip-flop having an output terminal and an input terminal, the input terminal being connected to the output terminal of the third multiplexer.

7. (Previously Presented) A communication system comprising:

a first device having a plurality of transceivers; and

a second device having a plurality of transceivers;

wherein the plurality of transceivers in the first device is connected to the plurality of transceivers in the second device which receives control signals for aligning data received from the first device; and

each of the transceivers comprises:

a buffer,

a first flip-flop that accepts a first input signal and generate an output signal;

a first multiplexer having an output terminal and at least a first and a second input terminal, the first input terminal accepting the output signal of the first flip-flop, and the second input terminal being connected to a second input signal;

a second flip-flop having an output terminal and an input terminal that connects with the output terminal of the first multiplexer;

a second multiplexer having an output terminal and at least a first and a second input terminal, the first input terminal being connected to the output terminal of the second flip-flop, and the second input terminal being connected to the second input signal; and

a third flip-flop having an output terminal to control the buffer and an input terminal, the input terminal being connected to the output terminal of the second multiplexer.

8. (Original) The system of claim 7 wherein each of the transceivers further comprises:

a third multiplexer having an output terminal and at least a first and a second input terminal, the first input terminal being connected to the first input signal, the second input terminal being connected to the second input signal; and

a fourth flip-flop having an output terminal and an input terminal, the input terminal being connected to the output terminal of the third multiplexer.

9. (Previously Presented) The system of claim 1 wherein the system for coordinating channel bonding operations of a plurality of transceivers comprises a system for aligning bytes of a word.

10. (Canceled)

11. (Previously Presented) The system of claim 1 wherein said transceivers comprise a plurality of levels, where each slave transceiver comprises an input to receive a control signal from a previous level.

12. (Previously Presented) The system of claim 11 wherein each slave transceiver is configured by mode control signal to receive a control signal from either a master transceiver or a slave transceiver.

13. (Previously Presented) The apparatus of claim 5 wherein the first input signal comprises a master input signal.

14. (Previously Presented) The apparatus of claim 5 wherein the second input signal comprises a control signal from a previous stage.

15. (Previously Presented) The apparatus of claim 5 wherein the output of said second multiplexer of a transceiver comprises a control signal for the transceiver.

16. (Previously Presented) The apparatus of claim 6 wherein the output of the fourth flip-flop of a transceiver comprises a control signal coupled to another transceiver.

17. (Previously Presented) The system of claim 7 wherein the communication system comprises N levels of devices having a plurality of transceivers.

18. (Previously Presented) The system of claim 17 wherein a path from an input of a control circuit of a master transceiver to an output of the control circuit generating a control signal coupled to the master transceiver comprises N flip flops.

19. (Previously Presented) The system of claim 18 wherein each level of transceivers following the master transceiver comprises N-X flip flops where X comprises the number of stages after the master transceiver.

20. (Previously Presented) The system of claim 19 wherein the communication system comprises a field programmable gate array.